

**WHAT IS CLAIMED IS:**

- 1     1.     A method for electrically stressing through a specified voltage at least one  
2     semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and  
3     reliability evaluation of product wafers, said method comprising:  
4             applying said voltage to said at least one chip for the probing thereof in  
5             the absence of physically contacting the chip surface; and  
6  
7             magnetically inducing said voltage to said at least one chip through the  
8             interposition of a mask onto which the voltage is induced and thereafter  
9             conducted to electrical contacts on said wafer.
- 1     2.     A method as claimed in Claim 1, wherein said applied voltage produces  
2     specified voltage bias conditions by inducing the voltage for a circuit utilizing a time  
3     varying magnetic field which is fixed with respect to said circuit.
- 1     3.     A method as claimed in Claim 2, wherein an electrical field which is  
2     represented by said induced voltage is based on Faraday's law setting forth that said  
3     voltage which is induced by a time rate of change of a magnetic field for said circuit  
4     which is fixed with respect to said magnetic field.
- 1     4.     A method as claimed in Claim 1, wherein said induced voltage is obtained at a  
2     top layer of said mask which is positioned on said wafer; and connections are made to  
3     said at least one chip by said mask for effectuating said burn-in without interference  
4     with the normal operation of said at least one semiconductor chip.
- 1     5.     A method as claimed in Claim 2, wherein said circuit comprises a loop  
2     defining an area on a wafer, said mask being positioned on said wafer so as to enclose  
3     said area and having electrical contacts for an induced voltage through said time  
4     varying magnetic field within said enclosed area.

1 6. A method as claimed in Claim 5, wherein said loop comprises a metallic line  
2 on said wafer forming an open circuit having electrical contact points provided at open  
3 ends of said circuit for producing said induced voltage.

1 7. A method as claimed in Claim 6, wherein said loop is of a rectangular  
2 configuration to define a generally rectangular area on said wafer.

1 8. A method as claimed in Claim 6, wherein said metallic line is constituted of  
2 copper.

1 9. A method as claimed in Claim 6, wherein said metallic line is constituted of  
2 aluminum.

1 10. A method as claimed in Claim 2, wherein said circuit comprises a circular  
2 magnetic core having an air gap for receiving said wafer with said at least one chip  
3 and said mask positioned thereon; and an electrical coil for energizing said magnetic  
4 core to produce said specified voltage bias conditions.

1 11. A method as claimed in Claim 10, wherein said voltage is supplied to said  
2 electrical energizing coil from a radio frequency voltage source.

1 12. A method as claimed in Claim 11, wherein said circular magnetic core is  
2 constituted of a Permalloy powder having a composition 2% by weight of *Mo*, 81% by  
3 weight of *Ni* with the remainder being iron and impurities.

1 13. A method as claimed in Claim 10, wherein said air gap receiving said wafer  
2 and mask is adapted to provide for the burn-in of differently sized wafers.

1 14. A method as claimed in Claim 10, wherein said electrical energizing coil  
2 consists of an isolated electrical wire comprised of copper wire strands.

1 15. A method as claimed in Claim 10, wherein said wafer and mask are retained in  
2 said air gap by a wafer holder consisting of a dielectric material.

1 16. A method as claimed in Claim 10, wherein said magnetic core includes a  
2 plurality of said circular magnetic cores interconnected by arms, and each said core  
3 having an air gap for receiving respectively a wafer and covering mask so as to  
4 facilitate the simultaneous controlled burn-in of a plurality of said wafers.

1 17. A method as claimed in Claim 2, wherein a rectangular core of non-magnetic  
2 material has electrical wire coils wound thereabout, said wire coils being connected to  
3 decal masks on a plurality of wafers positioned centrally on said core, each said decal  
4 mask being provided to conduct a generated voltage to a chip under said mask.

1 18. A method as claimed in Claim 17, wherein each said coil is conducted to a  
2 time varying voltage source so as to generate a magnetic field perpendicular to the  
3 surface of each said wafer in the center of said non-magnetic core.

1 19. A method as claimed in Claim 18, wherein electrical wires extend from each  
2 said mask to a panel for the direct measurements and verification of the direct voltages  
3 present on each of said wafer.

1 20. A method as claimed in Claim 17, wherein said non-magnetic core is  
2 constituted of wood.

1 21. A method as claimed in Claim 17, wherein at least nine wafers are positioned  
2 on each core for simultaneous burn-in thereof.

1 22. A method as claimed in Claim 1, wherein said mask comprises an interposer  
2 forming a decal on said wafer surface so as to protect the surface of said wafer from

3 direct contact with a probe during burn-in and voltage screening through electrical  
4 stressing.

1 23. A method as claimed in Claim 22, wherein said method conducts the generated  
2 burn-in voltage to said at least one chip when mountable on P+ silicon substrates.

1 24. A method as claimed in Claim 22, wherein said method conducts the generated  
2 burn-in voltage to said at least one chip when mountable on P- silicon substrates.

1 25. A method as claimed in Claim 22, wherein said interposer is formed for  
2 mounting the wafer on either P+ silicon or P- silicon substrates by the steps of:

3 fixing a polyimide film to a frame to fully cover said wafer;

4

5 depositing at least on layer of a metallic film onto the polyimide film;

6 patterning said metallic film to provide wiring lines extending to the

7 edge of said wafer to facilitate measuring the induced voltage;

8

9 removing exposed metallic layer material at the bottom of the vias and

10 depositing a further wiring line layer forming a ring wire loop on said

11 wafer which is connected to said first wiring lines to facilitate applying

12 an electrical bias to each said ring wire loop;

13

14 placing lead/tin bumps into each of said vias and connecting said

15 bumps to said further wiring lines; and

16

17 adjusting bump heights whereby the pattern of the bumps interiorly of

18 the decal mask is a mirror-image of wire bond pads or C4 connects on

19 the wafer chip which is to be burned-in.

1 26. A system for electrically stressing through a specified voltage at least one  
2 semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and  
3 reliability evaluation of product wafers, said system comprising:  
4 an arrangement for applying said voltage to said at least one chip for  
5 the probing thereof in the absence of physically contacting the chip  
6 surface; and  
7  
8 magnetically inducing said voltage to said at least one chip through the  
9 interposition of a mask onto which the voltage is induced and thereafter  
10 conducted to electrical contacts on said wafer.

1 27. A system as claimed in Claim 26, wherein said applied voltage produces  
2 specified voltage bias conditions by inducing the voltage for a circuit utilizing a time  
3 varying magnetic field which is fixed with respect to said circuit.

1 28. A system as claimed in Claim 27, wherein an electrical field which is  
2 represented by said induced voltage is based on Faraday's law setting forth that said  
3 voltage which is induced by a time rate of change of a magnetic field for said circuit  
4 which is fixed with respect to said magnetic field.

1 29. A system as claimed in Claim 26, wherein said induced voltage is obtained at a  
2 top layer of said mask which is positioned on said wafer; and connections are made to  
3 said at least one chip by said mask for effectuating said burn-in without interference  
4 with the normal operation of said at least one semiconductor chip.

1 30. A system as claimed in Claim 27, wherein said circuit comprises a loop  
2 defining an area on a wafer, said mask being positioned on said wafer so as to enclose  
3 said area and having electrical contacts for an induced voltage through said time  
4 varying magnetic field within said enclosed area.

1 31. A system as claimed in Claim 30, wherein said loop comprises a metallic line  
2 on said wafer forming an open circuit having electrical contact points provided at open  
3 ends of said circuit for producing said induced voltage.

1 32. A system as claimed in Claim 31, wherein said loop is of a rectangular  
2 configuration to define a generally rectangular area on said wafer.

1 33. A system as claimed in Claim 31, wherein said metallic line is constituted of  
2 copper.

1 34. A system as claimed in Claim 31, wherein said metallic line is constituted of  
2 aluminum.

1 35. A system as claimed in Claim 27, wherein said circuit comprises a circular  
2 magnetic core having an air gap for receiving said wafer with said at least one chip  
3 and said mask positioned thereon; and an electrical coil for energizing said magnetic  
4 core to produce said specified voltage bias conditions.

1 36. A system as claimed in Claim 35, wherein said voltage is supplied to said  
2 electrical energizing coil from a radio frequency voltage source.

1 37. A system as claimed in Claim 36, wherein said circular magnetic core is  
2 constituted of a Permalloy powder having a composition 2% by weight of *Mo*, 81% by  
3 weight of *Ni* with the remainder being iron and impurities.

1 38. A system as claimed in Claim 35, wherein said air gap receiving said wafer  
2 and mask is adapted to provide for the burn-in of differently sized wafers.

1 39. A system as claimed in Claim 35, wherein said electrical energizing coil  
2 consists of an isolated electrical wire comprised of copper wire strands.

1 40. A system as claimed in Claim 35, wherein said wafer and mask are retained in  
2 said air gap by a wafer holder consisting of a dielectric material.

1 41. A system as claimed in Claim 35, wherein said magnetic core includes a  
2 plurality of said circular magnetic cores interconnected by arms, and each said core  
3 having an air gap for receiving respectively a wafer and covering mask so as to  
4 facilitate the simultaneous controlled burn-in of a plurality of said wafers.

1 42. A system as claimed in Claim 27, wherein a rectangular core of non-magnetic  
2 material has electrical wire coils wound thereabout, said wire coils being connected to  
3 decal masks on a plurality of wafers positioned centrally on said core, each said decal  
4 mask being provided to conduct a generated voltage to a chip under said mask.

1 43. A system as claimed in Claim 42, wherein each said coil is conducted to a time  
2 varying voltage source so as to generate a magnetic field perpendicular to the surface  
3 of each said wafer in the center of said non-magnetic core.

1 44. A system as claimed in Claim 43, wherein electrical wires extend from each  
2 said mask to a panel for the direct measurements and verification of the direct voltages  
3 present on each of said wafer.

1 45. A system as claimed in Claim 42, wherein said non-magnetic core is  
2 constituted of wood.

1 46. A system as claimed in Claim 42, wherein at least nine wafers are positioned  
2 on each core for simultaneous burn-in thereof.

1 47. A system as claimed in Claim 26, wherein said mask comprises an interposer  
2 forming a decal on said wafer surface so as to protect the surface of said wafer from

3 direct contact with a probe during burn-in and voltage screening through electrical  
4 stressing.

1 48. A system as claimed in Claim 47, wherein said method conducts the generated  
2 burn-in voltage to said at least one chip when mountable on P+ silicon substrates.

1 49. A system as claimed in Claim 47, wherein said method conducts the generated  
2 burn-in voltage to said at least one chip when mountable on P- silicon substrates.

1 50. A system as claimed in Claim 47, wherein said interposer is formed for  
2 mounting the wafer on either P+ silicon or P- silicon substrates by means of:  
3 fixing a polyimide film to a frame to fully cover said wafer;  
4  
5 depositing at least on layer of a metallic film onto the polyimide film;  
6 patterning said metallic film to provide wiring lines extending to the  
7 edge of said wafer to facilitate measuring the induced voltage;  
8  
9 removing exposed metallic layer material at the bottom of the vias and  
10 depositing a further wiring line layer forming a ring wire loop on said  
11 wafer which is connected to said first wiring lines to facilitate applying  
12 an electrical bias to each said ring wire loop;  
13  
14 placing lead/tin bumps into each of said vias and connecting said  
15 bumps to said further wiring lines; and  
16  
17 adjusting bump heights whereby the pattern of the bumps interiorly of  
18 the decal mask is a mirror-image of wire bond pads or C4 connects on  
19 the wafer chip which is to be burned-in.